Comparison of Threshold Voltage Extraction Techniques on Ge FinFETs

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***Abstract*—This manuscript presents an analysis of the threshold voltage extracted from three different methods: constant current, linear extrapolation, and second derivative. All methods depend only on the drain/source current versus gate voltage transfer curve. The device under evaluation is the p-type germanium finFET from STI first process. Additionally, a long channel device is considered to prevent the short channel effect. Finally, both linear extrapolation and second derivative methods present the most accurate results.**

***Index Terms*—Fin width, High mobility material, Nanoeletronics, p-type channel, STI**

I. Introduction

In the last decades, many efforts have been given to shrink the Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) in order to increase the device density in the chip of a integrated circuit, following the Moore's law. However, the geometric reduction of the MOSFETs also implies on a critical issue, known as short channel effect (SCE) [1, 2]. One compromises the control of the depletion charges into the channel region by the gate terminal, since the distance between the drain and source regions also decreases, affecting the gate controllability due to the SCE [3]. Therefore, the fin Field-Effect Transistors (finFETs), which is one of the multiple-gate structures, have been extensively studied and introduced in the industry for scaled CMOS/memory applications [2, 4]. In addition, these devices present a more improved electrostatic coupling [5], resulting in a better control of the SCE [2]. A few leading-edge manufacturers have launched high-κ dielectric and metal gate (HKMG) products using gate-first and gate-last process-flow. Intel has been the first company to use HKMG in its 45-nm technological node products and has also launched the first 22-nm finFETs on the market: in its Ivy Bridge microprocessor [6].

Currently, many studies are being concentrated on finFETs, mainly on germanium (Ge) p-type channel transistors, due to its higher channel carrier mobility when compared to silicon (Si), which is suitable for future high performance circuits [7, 8]. Additionally, Ge presents greater bulk hole mobility among the other semiconductor materials, turning it as the most promising material for p-FET devices [9]. In this context, the Ge devices can be epitaxilly grown on Si substrate, however, for this heteroepitaxy layers, there are a few strategies that must be adopted to reduce the influence of the defects in the MOSFET channel, as reported in [9–11]. Those defects, such as threading dislocations (TD) and misfit dislocations (MD), cause damage to the Si/Ge interface due to the lattice mismatch and the different thermal coefficients of materials [9, 12, 13]. Additionally, a few device electrical parameters, such as the threshold voltage (V_{TH}) [13], can be affected by the excess noise generation-recombination of carriers induced by the TD [12].

The V_{TH} is a key parameter for enhanced channel MOSFETs and it can be associated to the minimum gate voltage value to form a channel layer between drain and source. This parameter is necessary for several transistor design metrics and process parameters and it can also be affected by the SCE [14]. In this context, this work presents the partial results from a scientific initiation project, which focuses on comparing three known extraction methods of V_{TH} among other ones previously reported in [15] for the 10 μm long germanium finFETs, considering different fin widths. Additionally, a first order analysis is conducted regarding the already reported W_{fin} dependence on V_{TH} for the finFET experimental data [16].

II. Germanium p-channel finFETs

This section focuses on identifying the main features of a finFET, the device characteristics and measurements specifications.

A. Structure

Fig. 1 shows the basic three-dimensional structure of a finFET. The geometric dimensions are L, which represents the length of the channel, W_{fin} that is the fin width, and H_{fin} determines the fin height of the finFET. The effective width W_{eff} of the finFET structures is multiple of W_{fin} and can be increased using multiple fins (n) in parallel. Mathematically, W_{eff} is represented by $n(W_{fin}+2H_{fin})$. There are two types

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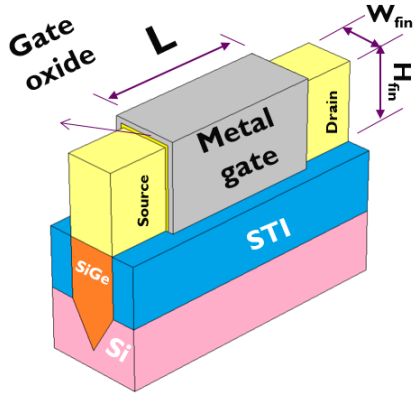

Fig. 1. Basic schematic of a finFET structure.

TABLE I
CHARACTERISTICS OF THE ANALYZED GE FINFETS.

Parameter	Value/characteristic
$Si_{1-x}Ge_x$	x = 70 %
t_{ox} (nm)	1 nm of SiO_2 + 1.8 nm of HfO_2
Metal gate (nm)	5 (composition TiN)
W_{fin} (nm)	20; 30; 50 and 100
H_{fin} (nm)	30
L (nm)	10,000
Fins in parallel	4
Channel doping concentration	1×10^{15} cm^{-3} (non-intentionally doped)
Substrate doping concentration $Si_{1-x}Ge_x$	5×10^{18} cm^{-3} (dopant: phosphorus)

of substrate that can be employed for MOSFET fabrication: bulk and Silicon-on-Insulator (SOI) wafers [17].

B. Device Characteristics

This work is based on an experimental study of germanium p-finFETs, which were fabricated at Imec, Belgium. These devices were manufactured on a 300 mm silicon wafer, using a shallow trench isolation (STI) first process, and their main characteristics are shown in Table I.

The current-voltage (I-V) characteristic curves were measured by using a semiconductor device parameter analyzer. The voltage applied to the gate terminal (V_G) was varied from the accumulation to inversion regime, stepped by 20 mV, under a fixed drain voltage value of V_D = –50 mV, i.e., low lateral electric field, and at room temperature [18].

III. FINFET THRESHOLD VOLTAGE

For p-channel planar MOSFET devices, the concentration of free carriers (holes) in the inversion layer is equal to the concentration of electrons in the substrate when V_G reaches V_{TH} value. At this point, the surface potential of the structure (ϕ_S) is approximately to twice the Fermi level (ϕ_F) value [3, 17]. However, for finFETs, the inversion charge layer is quite limited when the surface potential is at $2\phi_F$, then, at the beginning of the strong inversion, the surface potential is slightly greater than $2\phi_F$ [19]. The value of the finFET threshold voltage can be obtained by [19]

$$V_{TH} = \frac{Q_D}{C_{OX}} + 2\phi_F + \phi_{MS} - \frac{Q_{SS}}{C_{OX}} + V_{inv}, \quad (1)$$

$$Q_D = \frac{qN_D W_{fin}}{2}, \quad (2)$$

where Q_D is related to the depletion charge density into the channel region, N_D is the channel doping concentration of semiconductor acceptor impurities, W_{fin} is the fin width, ϕ_{MS} refers to the difference of work function, in V, between the metal and the semiconductor, which does not depend on the biasing, but only on the physical characteristics, Q_{SS} represents the fixed and mobile charges into the gate dielectric layer, C_{OX} is the gate capacitance density, and V_{inv} is the additional surface potential at $2\phi_F$ for finFETs, which the narrower the fin and lower the concentration of dopants, the higher the value of V_{inv} [19].

IV. THRESHOLD VOLTAGE EXTRACTION METHODS

The evaluated extraction methods depend on the input characteristic of the devices: drain current (I_D) as a function of gate voltage (V_G) that is illustrated in the Fig. 2. Additionally, both subthreshold and strong inversion regions are indicated.

A. Linear-Extrapolation (LE)

The linear extrapolation (LE) method is one of the most used to determine the value of the V_{TH}. It is based on plotting the I_D x V_G and g_m x V_G curves, followed by establishing an inflection point on the I_D curve, where the transconductance (g_m) curve has its maximum value. From that point, a tangent line must be drawn and extrapolated to the horizontal axis. The point of intersection of this line with the x-axis is the value of V_{TH} [14, 15, 20].

The LE method is affected by second-order effects, such as the mobility degradation and the series resistances that affects the maximum inflection point [15].

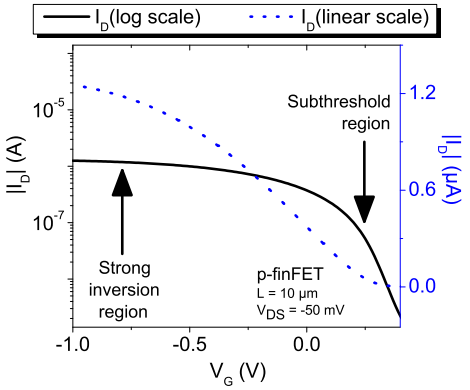

Fig. 2. Drain current as function of gate voltage for both linear and logarithmic scales.

B. Constant-Current (CC)

In [14, 15], it is suggested that the threshold voltage value can be found from the I_D vs. V_G curve at an absolute V_D value lower than 100 mV, that is low lateral electric field. The value of V_{TH} is defined arbitrarily at a point on the curve where, on the x-axis (V_G), for a I_D value equivalent to (W_{eff}/L)$\times 10^{-7}$, in A.

This method is advantageous for its simplicity. Furthermore, the value found for the threshold voltage can also undergo more changes due to the effects caused by parasitic resistances and mobility degradation [15].

C. Second-Derivative (SD)

This method consists of taking the second derivative of the drain current with respect to gate voltage ($\partial^2 I_D/\partial V_G^2$) and extracting the V_G value (x-axis), corresponding to the maximum value of the generated curve (y-axis). The derivative technique can be understood from the analysis of the I_D dependence on V_G from exponential to linear/quadratic regime. In other words, this technique observes the change from the diffusion mechanism (V_G below V_{TH}) to the drift mechanism (V_G above V_{TH}). Thus, for V_G value greater than V_{TH}, the channel is formed for the current flow, a peak will occur exactly in V_G = V_{TH}, where the device goes from the off-state to the strong inversion regime. [15, 20].

One of the issues within this method is that it can be noisy, since the difference between one point and another is amplified when it is derived twice. However, it is possible to use mathematical filters to perform the second derivative in order to smooth the curves. This extraction technique has the advantage of avoiding the effects of the series resistance [15].

V. Results and Discussions

Fig. 3 shows the threshold voltage as a function of the fin width for a channel length of 10 μm, considering the three discussed methods. It is worth mentioning that this result has been reported in [16], taking into consideration one of these extraction methods. For all devices, similar behavior among the methods is observed, as the fin width decreases, the threshold voltage increases, except for W_{fin} of 50 nm. In this case, a second-order effect might play a role, since this behavior is not found in STI last process devices as previously reported in [16]. Despite of the similarity trends of the curves, the SD and LE methods have lower (and similar) values for V_{TH} compared to the CC one.

In order to inspect the contribution of the fin width on V_{TH} by the presented model from (1), it was calculated the V_{TH} values for different fin widths, assuming ϕ_F of –0.0966 V and ϕ_{MS} of 0.2666 V. At a first order analysis, the Q_{SS} and V_{inv} were neglected in the calculations. The results are approximately 0.073 V for all evaluated widths, implying on an insignificant contribution of around a few µV, as W_{fin} value increases. Therefore, it can be considered that the depletion charge density (Q_D) contribution is negligible, as long as the channel doping concentration is non-intentionally doped (1×10^{15} cm^{-3}), constant values for ϕ_F and ϕ_{MS}, and assuming Q_{SS} and V_{inv} as null values. Thus, since the fin width does not significantly influence the result, other hypotheses can be raised for the threshold voltage shifting illustrated in Fig. 3.

The fact that the V_{TH} values are positive for studied p-type devices (in Fig. 3) indicates that the effective metal work function may not be enough to shift V_{TH} for negative values. Another reason for V_{TH} to shift in the positive direction of V_G is the existence of a thin layer of SiO_2 from the gate dielectric stack that acts as an electrical dipole [21]. The last hypothesis could be the influence of trap density at the channel/gate oxide interface that might affect the Q_{SS} parameter from (1).

The relative error in percentage ($\epsilon_{rel(\%)}$) is used in order to compare the results of the extracted V_{TH} from different methods with each other. It can be calculated from

$$\epsilon_{rel(\%)} = 100\frac{|V_{true} - V_{approx}|}{V_{true}}, \quad (3)$$

where the obtained V_{TH} by the SD method is assumed as true value (V_{true}) and the threshold voltage of the other two methods, as approximate value (V_{approx}). Therefore, two

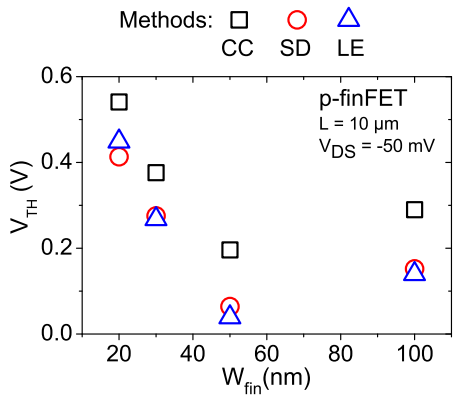

Fig. 3. Threshold voltage as a function of fin widths for different extraction methods.

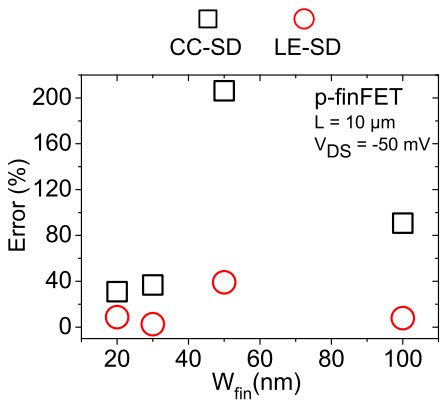

Fig. 4. Relative error of the threshold voltage, in percentage, assuming V_{TH} of the SD method as the true value, in relation to the V_{TH} of the methods: (A) CC and (B) LE.

percentage relative errors are considered: (A) between the constant current and the second derivative methods; and (B) between the linear extrapolation and the second derivative ones.

From Fig. 4, it can be noted that the error between the CC and SD methods is greater compared to the one of the LE and SD methods. For the (B) case, the error remains practically constant and with values always significantly lower than (A). Additionally, error (A) tends to become even greater as the dimensions of the device are increased. Therefore, while the SD and LE methods have a similar trend, the CC one seems to be less reliable for wider devices.

VI. Conclusion

In this paper, three techniques were studied for extracting a key electrical parameter for finFETs, the threshold voltage. Although there are a considerable difference among the obtained V_{TH} values for the three evaluated methods, reaching up to 0.2 V for the same device, in all case, the fin width dependence on this parameter is obviously identified. Thus, the overall effect on the devices can be observed independent of the method. On the other hand, from a practical point of view, the second derivative and linear extrapolation methods might require extra data processing. However, they seem to be more reliable than the constant current one, since their values are quite close to each other.

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